REMARKS/ARGUMENTS

Favorable reconsideration of this application, in light of the following discussion, is respectfully requested.

Claims 1-26 are currently pending and the Title is amended to more clearly indicate the claimed subject matter.

In the outstanding Office Action, Claims 7 and 20 are rejected under 35 U.S.C. § 102(e) as anticipated by Okamoto et al. (U.S. Patent No. 6,774,674, hereinafter "Okamoto"); Claims 8-12 and 21-26 are indicated as allowable if rewritten in independent form; Claims 1-6 and 13-19 are indicated as allowable.

Applicant and Applicant's representative greatly appreciate the indication of allowable subject matter, and the courtesy of a personal interview with the Examiner on October 11, 2005. During the interview, differences between the present invention and references in the outstanding Office Action were discussed. Comments discussed during the interview are reiterated below.

Applicant respectfully traverses the rejection of Claim 7 under 35 U.S.C. § 102(e) as anticipated by Okamoto.

Claim 7 is directed to a semiconductor device that includes, in part:

> a high potential part including a control part configured to control conduction/non-conduction of a high side switching device which is one of said first and second switching devices;
>
> a reverse level shift part configured to level-shift a signal from said high potential part to supply the level-shifted signal to a low side logic circuit operating on the basis of said low main power potential; and
>
> a voltage detecting device provided in said high potential part and configured to detect a potential at an output line of said reverse level shift part and to supply a logic value based on said potential for said control part, thereby causing said control part to control conduction/non-conduction of said high side switching device.

Claim 20 recites analogous features regarding at least the voltage detection device provided in the high potential part.

By way of background a high voltage integrated circuit (HVIC) device may be used as a gate driver for a power transistor such as an integrated gate bipolar transistor (IGBTs). IGBTs may be used to perform power line bridge rectification and may be positioned so that a high side IGBT and a low side IGBT are turned on together. These IGBTs may be damaged when certain current conditions occur causing a current "shoot through" problem.[1]

In a non-limiting example, Figure 25 shows a semiconductor device including PMOS transistor 23 serving as a voltage detector (e.g., voltage detecting device), having a gate electrode connected to a drain electrode of HPMOS transistor 51 provided in the high side power device driving circuit HD (e.g., in said high potential part), which enables detecting of the potential VS by monitoring potential V3.[2] PMOS transistor 23 allows the potential VS to be monitored within the high side power device driving circuit HD (e.g., a voltage detecting device in said high potential part).[3]

In other words, the inventions of Claims 7 and 20 employ a voltage detection feature at the high part of the circuit to detect a potential at an output line of the reverse level shift part.

As discussed during the interview, Okamoto fails to teach or suggest each feature of independent Claims 7 and 20. Further, as discussed during the interview, Applicant respectfully traverses the association in the outstanding Office Action that Okamoto discloses a voltage detection device provided in said high potential part.[4] Okamoto attempts to prevent damage to a power transistor without having a voltage detection device provided in a high

[1] Specification, page 1 lines 9-17.
[2] Specification, page 35, line 1 to page 36, line 20.
[3] Specification, page 35, line 1 to page 36, line 20.
[4] Office Action of September 9, 2005, page 3, lines 3-10.

potential part. All examples described in Okamoto include a level shifting circuit[5] that employs a timing control to decrease a chance of damage.[6] Further, Okamoto attempts to prevent a malfunction of a power device by employing a level shifting circuit[7] that includes a timing control mechanism to limit a time that both devices are in "on" states.[8] The "on" states are limited to correspond to a cycle of first and second iterative pulse signals at a maximum value followed by normal control to prevent the devices from being simultaneously turned on and inconveniently shorted.[9] Okamoto's timing control device or level shifting circuit is different than a voltage detection device.

Therefore, Applicant respectfully submits that Okamoto fails to teach or suggest every feature recited in Claim 7 and Claim 20. Specifically, Okamoto fails to teach or suggest "a voltage detection device provided in said high potential part," as recited in Claims 7 and 20.

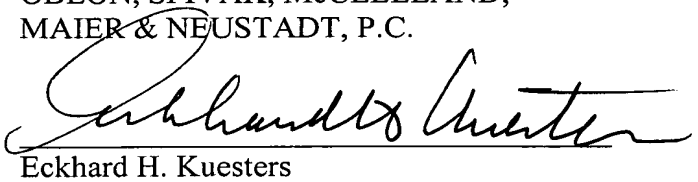
Accordingly, Applicant respectfully submits that independent Claims 7 and 20, and claims depending therefrom, are allowable.

[5] Okamoto, col. 6 line 15 to col. 28, line 44.
[6] Okamoto, col. 6-28.
[7] Okamoto, col. 3, lines 39-42.
[8] Okamoto, col. 4, lines 9-15.
[9] Okamoto, col. 4, lines 9-15 and col. 4, lines 16-62.

Consequently, in view of the foregoing discussion, it is respectfully submitted that the application is in condition for allowance. An early and favorable action is therefore respectfully requested.

Respectfully submitted,

OBLON, SPIVAK, McCLELLAND,
MAIER & NEUSTADT, P.C.



Eckhard H. Kuesters
Attorney of Record
Registration No. 28,870

Zachary S. Stern
Registration No. 54,719

Customer Number
22850

Tel: (703) 413-3000
Fax: (703) 413 -2220
(OSMMN 06/04)